34.6 Thyristor-Based Volatile Memory in Nano-Scale CMOS

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Thyristor is well-known for its high-current drive capability and its bi-stable characteristics. It has been widely used in power-electronics applications. With the exponential advances in CMOS technology and the emergence of SOI and FinFET technologies, tiny thyristor devices can now be easily embedded into conventional nano-scale CMOS. This enables the creation of a memory cell technology with features that include small cell size, high performance, reliable device operation, and good scalability. There has always existed a fundamental performance-density trade-off between SRAM and DRAM, the only two commercially viable volatile memory technologies of the past twenty-five years. SRAM provides high performance at the expense of a large cell area, while DRAM provides high density but with low performance. For networking and L2/L3 Cache applications in particular, there is a huge demand for RAM that combines the highest possible random cycle performance with the highest possible density. Thyristor-based RAM (T-RAM) is a volatile memory technology that breaks through the performance-density trade-off of conventional DRAM and SRAM by providing SRAM-like performance and functionality at 2× to 3× the chip/macro density (Fig. 34.6.1).

The performance limitation of DRAM is primarily a result of using a passive capacitor as the storage device without an internal gain. DRAM read operation is therefore destructive and the data retention is highly leakage sensitive. Destructive read requires the use of a read and write-back operation for every memory access or refresh operation, slowing down the random cycle time. A T-RAM cell uses a bi-stable storage mechanism that is the result of the internal regenerative gain of a cross-coupled PNP-NPN bipolar transistor pair (inherent in thyristor device structure), providing non-destructive read and self-recovering cell restore (Fig. 34.6.2). Restore is the application of periodic short pulses to cell WL1 to self-recover the stored cell data while minimizing its standby power. Since a T-RAM cell consists of only two elements (a thyristor device and an access FET), its cell area is significantly smaller than 6T SRAM. The slow turn-off speed of a conventional thyristor is addressed in a T-RAM cell through the use of a thyristor structure, called thin capacitively coupled thyristor (TCCT). The viability and manufacturability of the T-RAM memory technology is demonstrated in a commercial 0.13µm SOI logic technology, using logic-based design rules in the cell and with the simple addition of photo-mask/implant steps. A T-RAM cell size of 0.562µm^2 is achieved, which is more than 4-times smaller than published 0.13µm 6T-SRAM cell sizes [1].

Some of the design attributes of the T-RAM technology are shown in Figs. 34.6.3 and 34.6.4, which show the basic cell array organization and timing diagram. The output read current of the bit cell is single-ended and the BL is precharged to ground prior to the read operation. When the cell stores a "0", (i.e. the thyristor is in high-resistance off-state and provides no current), the BL remains at the pre-charged V_{SS} level. When the cell stores a "1", the cell provides 35 to 40µA of read current to pull the BL up from the precharged V_{SS} state. A separate reference voltage level midway between the grounded "0" level and the "1" level is provided separately to the other input of the sense amp. Due to the compact layout of the cell array, there is a significant coupling capacitance between the adjacent BLs. If the targeted cell to be read is a "0" while both adjacent BLs are being read as "1", the "0" BL can couple up significantly, greatly increasing the necessary reference voltage level, and consequently, pushing out the read time substantially. This effect is overcome by a shielding technique, whereby every other BL is held at ground level, while the interleaved BLs are read. There is, however, a characteristic of the write operation that is in conflict with this shielding technique. When WL2 is pulsed high to write the target memory cells, it over-writes all cells connected to the same WL2 with the current state of their BLs non-selectively. Therefore, since all contiguous bit lines are written during a given WL2 pulse while only every other BL can be read simultaneously, there must be a pre-read cycle of the interleaved half of the bits that are not intended to be read. For example, write operation on even BLs is preceded by a pre-read of odd BLs (see the second cycle in the timing diagram). Since T-RAM restore operation is fast (~0.5ns) and unlike DRAM refresh does not require external read and write-back, it is easily hidden as a dedicated slot at the end of each access cycle, so that SRAM-like functionality is maintained up to very high random cycle frequencies.

A 9Mb T-RAM test chip with full SRAM functionality that implements the proposed design aspects is demonstrated. Figure 34.6.5 shows the measured characteristics of the 9Mb T-RAM test chip. Figure 34.6.7 shows the die micrograph as well as the test-chip organization. A T-RAM cell random read/write speed of less than 2ns is demonstrated in silicon, which is comparable to 6T-SRAM, and significantly faster than typical read/write speed of DRAM. Measured power numbers from a 9Mb memory chip for 3 different modes are included. The standby power component due to restore is 18mA for the 9Mb test chip.

Architectural design improvements, currently in development for 0.13µm technology, are expected to provide improved read speed due to 4× improvement in signal generation time within the same area. Future implementations of the T-RAM technology are aligned with the future trends in MOS technology (Fig. 34.6.6). Various forms of SOI or FinFET technologies are being widely considered as critical technologies for scaling CMOS in deep nano-meter era. T-RAM cell technology can be integrated into such SOI or FinFET technologies by extra photo-mask/implant steps (added process cost <10%). The down-scaling of the silicon thickness in the future SOI and FinFET technology generations provides further improvement in the write performance of a T-RAM cell. It is expected that the current 4× cell area advantage of SOI T-RAM versus 6T-SRAM is maintained over multiple generations. A future 1T TCCT DRAM cell concept can further increase the density advantage of the T-RAM technology over 6T-SRAM while maintaining greater than 1GHz fully random access cycle times [2].

References:

[1] F. Nemati, et al., "Fully Planar 0.562µm^2 T-RAM Cell in a 130nm SOI CMOS Logic Technology for High-Density High-Performance SRAMs," *IEEE International Electron Device Meeting*, pp. 273-276, Dec., 2004.

[2] H.J. Cho, et al., "A Novel Capacitor-Less DRAM Cell Using Thin Capacitively-Coupled Thyristor (TCCT)," *IEEE International Electron Device Meeting*, paper 13.2, Dec., 2005.

[3] F. Morishita, et al., "A 312-MHz 16-Mb Random-Cycle Embedded DRAM Macro with a Power-Down Data Retention Mode for Mobile Applications," *IEEE J. Solid-State Circuits*, pp. 204-207, Jan., 2005.

[4] H. McIntyre, et al., "A 4-MB On-chip L2 Cache for a 90-nm 1.6-GHz 64-bit Microprocessor," *IEEE J. Solid-State Circuits*, pp. 52-59, Jan., 2005.

[5] G. Muller, et al., "Status and Outlook of Emerging Nonvolatile Memory Technologies," *IEEE International Electron Device Meeting*, pp. 567-570, Dec., 2004.

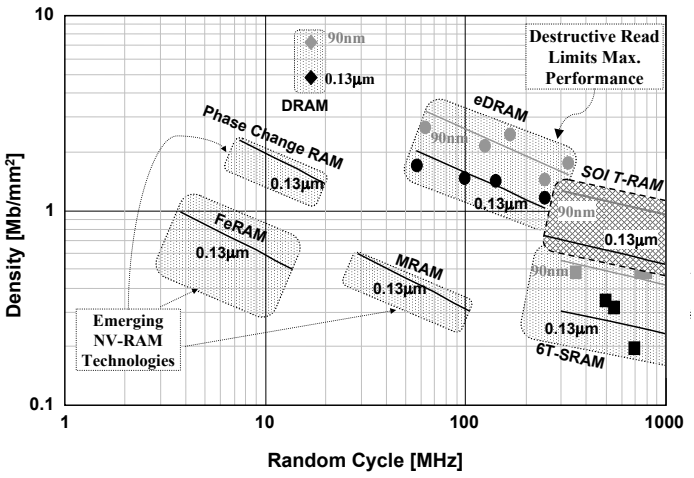

Figure 34.6.1: Performance-density trade-off among various RAM technologies.

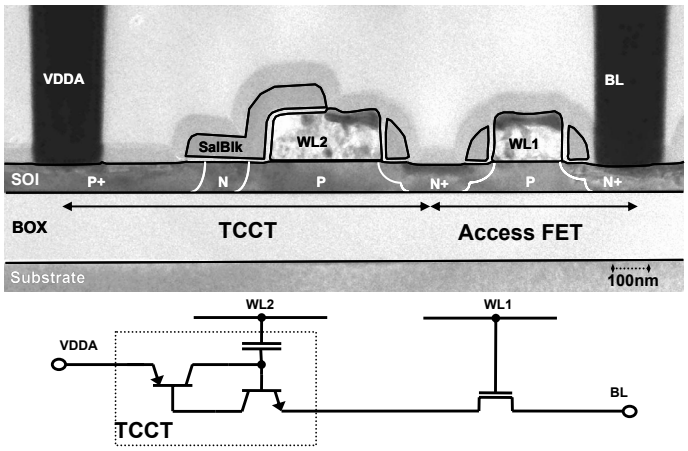

Figure 34.6.2: Cell cross-section and circuit model of 0.13µm planar SOI T-RAM cell.

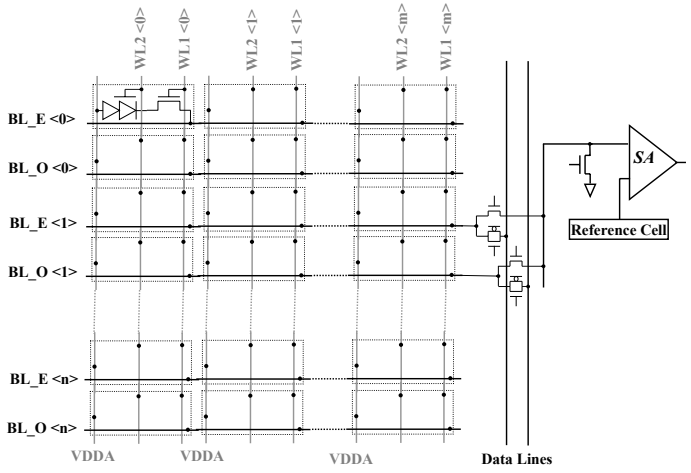

Figure 34.6.3: Basic T-RAM cell array organization.

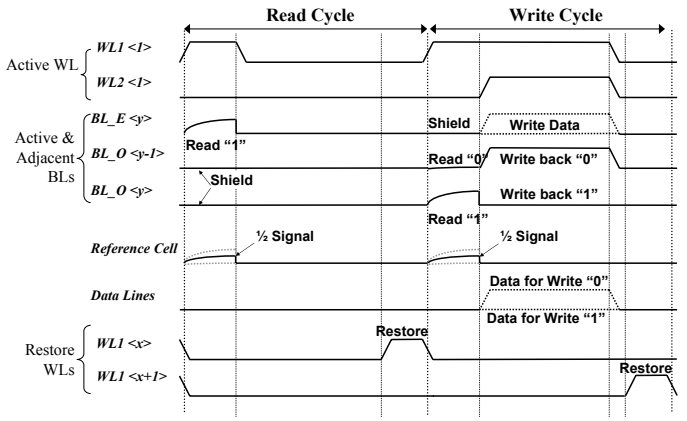

Figure 34.6.4: Basic read/write timing diagram showing BL shielding and pre-read.

Technology	130nm SOI Logic
Cell Area	1.56µm x 0.36µm = 0.562µm²
Supply Voltages	V_{DD}/V_{SS} (Logic, BL, WL1) = 1.2V/0V VDDA = 1.8V V_{DD}/V_{SS} (WL2)= 1.2V/-1.7V
Test Chip	512k x 18 = 9Mb, 19mm²
Speed – Read (WL1_H to Data_Latch)	1.6ns for 9Mb @105C
Speed – Write (WL2_H to WL1_L)	2ns for 9Mb @105C
Power – Active	0.68mA/MHz for 9Mb @0°C
Power – Standby, Restore	18mA for 9Mb @105°C
Power – Standby, Periphery / Leakage	33mA for 9Mb @105°C

Figure 34.6.5: Measured characteristics of 0.13µm 9Mb SOI T-RAM test chip.

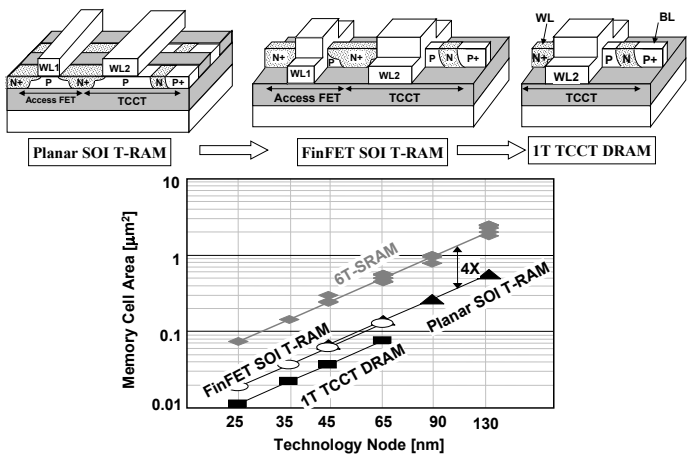

Figure 34.6.6: Future T-RAM cell technology direction.

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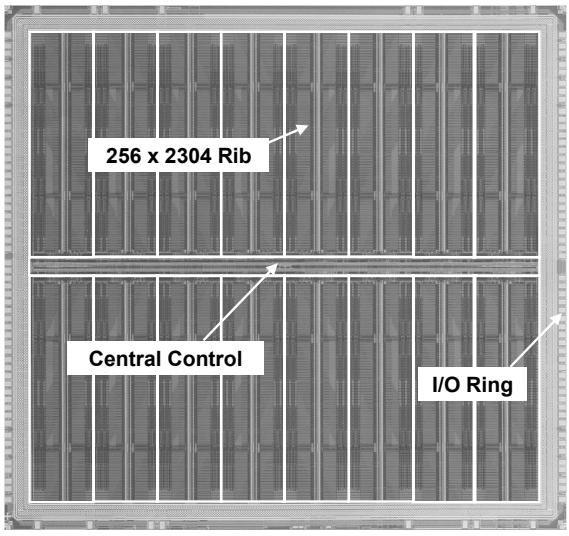

Figure 34.6.7: T-RAM 9Mb (512k×18) test-chip organization and die micrograph.

